

Hall Ticket Number:

| | | | | | | | | | | | | | | | | | | | |
|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| | | | | | | | | | | | | | | | | | | | |
|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|

Code No. : 15344 S O

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS), HYDERABAD

Accredited by NAAC with A++ Grade

B.E. (E.E.E.) V-Semester Supplementary Examinations, June-2023

Microprocessors and Microcontrollers Applications

Time: 3 hours

Max. Marks: 60

Note: Answer all questions from Part-A and any FIVE from Part-B

Part-A (10 × 2 = 20 Marks)

| Q. No. | Stem of the question | M | L | CO | PO |
|----------------------------------|--|---|---|----|-------|
| 1. | If the 8086 data segment Register Contains 4000H. What Physical address will the instruction MOV AL,[234BH] read ? What is the name of the addressing Mode for the above Instruction? | 2 | 2 | 1 | 1,3 |
| 2. | Describe the difference between the instructions MOV AX,2437H and MOV AX,[2437H] and name the addressing Modes of these instructions | 2 | 1 | 1 | 1,3 |
| 3. | Explain the following Assembler Directive with and example i)EQU ii) ORG | 2 | 1 | 2 | 2,3,5 |
| 4. | Explain the difference between ROL and RCL instructions | 2 | 1 | 2 | 2,3,5 |
| 5. | How many 128*8 RAM chips are needed to provide a memory capacity of 2048 bytes ? A)8 B)16 C)24 D)32 | 2 | 2 | 3 | 1,3 |
| 6. | Explain the purpose of HOLD and HLDA Pins in 8086 | 2 | 1 | 3 | 1,3 |
| 7. | How are the bits of the register PSW affected if we select Bank2 of 8051? A) PSW.5=0 and PSW.4=1 B) PSW.2=0 and PSW.3=1 C) PSW.3=1 and PSW.4=1 D) PSW.3=0 and PSW.4=1 | 2 | 1 | 4 | 2,3,5 |
| 8. | On power up, the 8051 uses which RAM locations for register R0- R7 A) 00-2F B) 00-07 C) 00-7F D) 00-0F | 2 | 1 | 4 | 2,3,5 |
| 9. | What is the default value of stack once after the system undergo the reset condition? A) 07H B) 08H C) 09H D) 00H | 2 | 1 | 4 | 2,3,5 |
| 10. | What kind of PSW flags remain unaffected by the data transfer instructions? A) Auxillary Carry Flags B) Overflow Flags C) Parity Flags D) All of the above | 2 | 1 | 4 | 2,3,5 |
| Part-B (5 × 8 = 40 Marks) | | | | | |
| 11. a) | With the help of neat block diagram, describe the functionality of Bus interface unit and Execution unit of 8086 μP | 4 | 3 | 1 | 1,2 |
| b) | Draw and explain the flag register of 8086 microprocessor | 4 | 2 | 1 | 1,2 |

| | | | | | |
|--------|---|---|---|---|-------|
| 12. a) | Write an Assembly Language Program to move a string from one location to another location in the same segment memory | 4 | 4 | 2 | 1,3 |
| b) | Differentiate between Procedure and Macro with an Example | 4 | 2 | 2 | 1,3 |
| 13. a) | Explain the Block Diagram of USART (8251) | 4 | 3 | 3 | 2,3,5 |
| b) | The 8255 Shown in Fig, Find | 4 | 4 | 3 | 2,3,5 |
| a) | Find the Port address for the Figure shown | | | | |
| b) | Find The Control Word if PA = OUT, PB = IN, PC0-PC3 = IN and PC4-PC7 = OUT | | | | |
| c) | Program the 8255 to get Data from PORTA and Send it to PORTB. In addition, data from PCL (PORT C Lower) is send out to the PCU (PORT C Upper). | | | | |
| | | | | | |
| 14. a) | List the Various Addressing Modes in 8051 and Explain them with an Example | 4 | 2 | 4 | 2,3,5 |
| b) | Explain pin configuration with circuit diagram for all port of 8051 microcontroller. | 4 | 2 | 4 | 2,3,5 |
| 15. a) | Explain different modes of Timer for 8051 microcontroller. | 4 | 2 | 4 | 2,3,5 |
| b) | Explain interfacing of stepper motor with microcontroller. Write program to rotate stepper motor in clockwise direction continuously in full step mode. | 4 | 4 | 4 | 2,3,5 |
| 16. a) | Draw and Explain Minimum Mode Block Diagram of 8086 | 4 | 3 | 1 | 1,2 |
| b) | Mention any four Data Transfer Instructions of 8086 with Examples | 4 | 2 | 2 | 1,3 |
| 17. | Answer any <i>two</i> of the following: | | | | |
| a) | Draw and explain 8086 Interrupt vector table | 4 | 4 | 3 | 2,3,5 |
| b) | List all the registers used in 8051 microcontroller in brief | 4 | 2 | 4 | 2,3,5 |
| c) | Write 8051 based assembly Program to generate a square wave on P1.0 of 10Khz frequency and 50% duty cycle. | 4 | 4 | 4 | 2,3,5 |

M : Marks; L: Bloom's Taxonomy Level; CO; Course Outcome; PO: Programme Outcome

| | | |
|------|-------------------------------|-----|
| i) | Blooms Taxonomy Level – 1 | 20% |
| ii) | Blooms Taxonomy Level – 2 | 40% |
| iii) | Blooms Taxonomy Level – 3 & 4 | 40% |
